ORGANIC CLASS Y SYSTEM-IN-PACKAGE TECHNOLOGY DEVELOPMENT

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Organic Class Y SiP Technology Development

Agenda

- Package Technology Roadmap for Space
  - System-in-Package technology definitions
- Fine Pitch Flip Chip on Organic Development
  - Program overview, status and results
- System-in-Package Technology Development
  - Program introduction and status
- Physics-of-Failure Reliability Modeling
  - Solder fatigue mechanism

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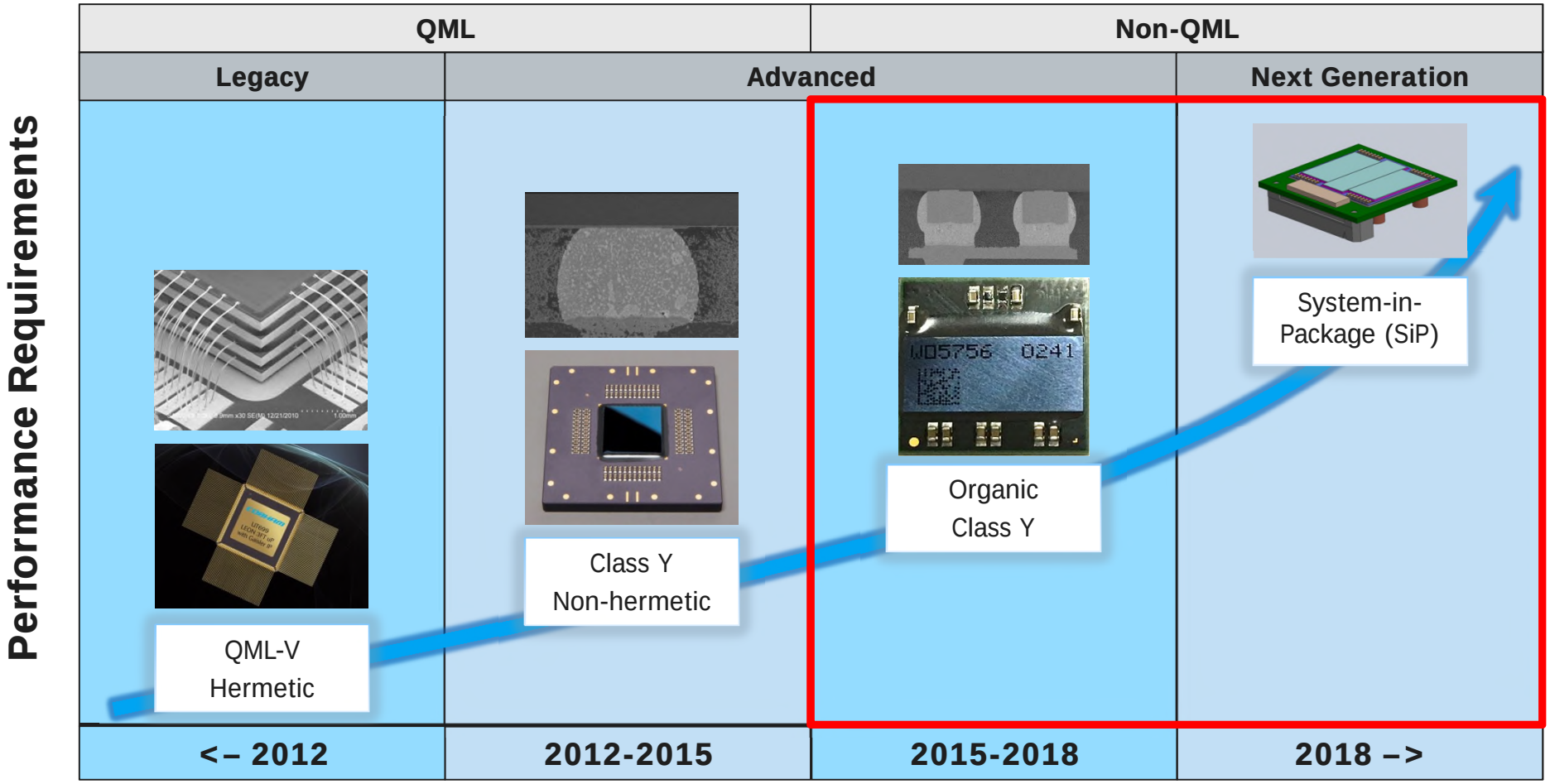
Cobham Package Technology Roadmap for Space Applications



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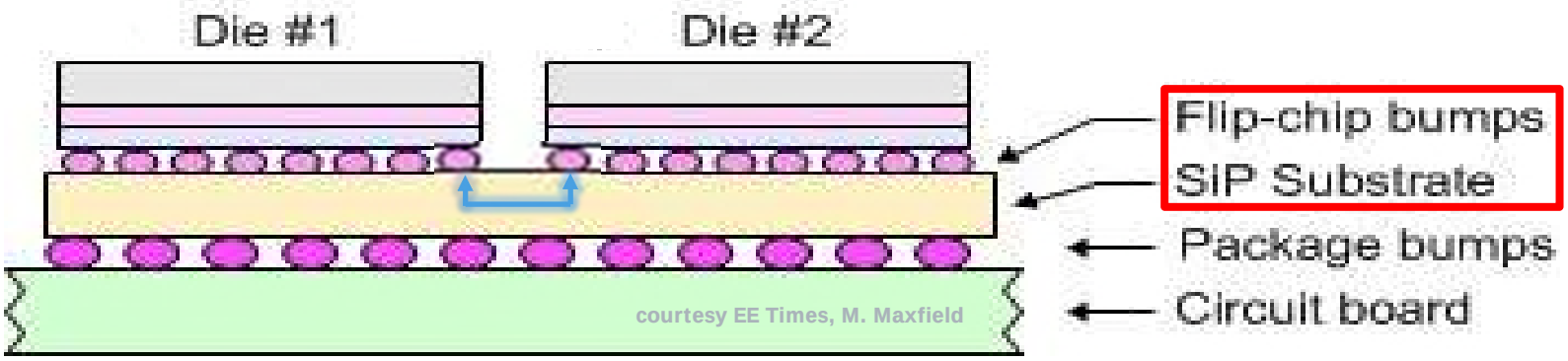
2.1D System-in-Package Technology



- *2.1D SiP technology allows for integration of hetero or homogeneous devices through the organic substrate*
  - Higher density integration compared to flip chip on organic BGA technology
  - Multiple die integrated through organic substrate
  - Advanced organic build-up substrate technology with fine lines and spaces
  - Copper pillar flip chip interconnects
  - Ball Grid Array second level interconnects

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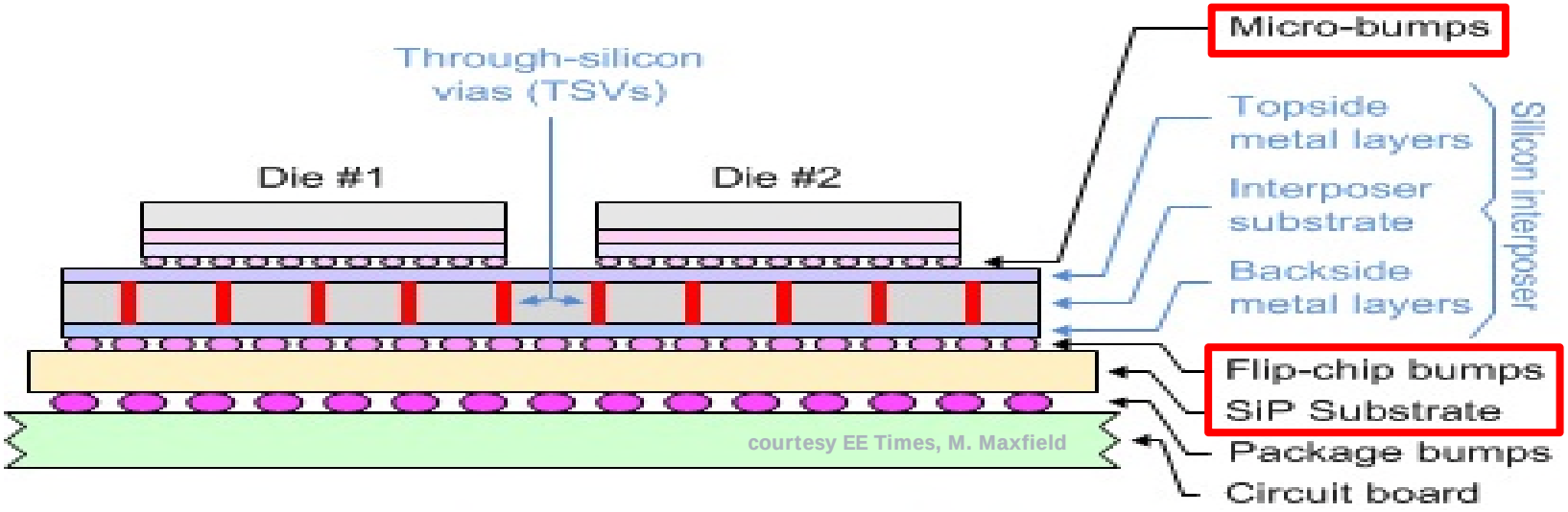
2.5D System-in-Package Technology



- *2.5D SiP technology provides a high density platform for integration of hetero and/or homogeneous devices*
  - Allows for devices to be partitioned (i.e., disaggregated) into discrete parts fabricated in disparate technologies, optimizing functionality and yield
  - Interposers technology utilizing through silicon vias (or glass)
  - Short interconnects lengths through interposer (e.g., between memory and logic devices) increase speed and reduce parasitics, power and size
  - Utilizes copper pillar and micro-bump flip chip interconnects

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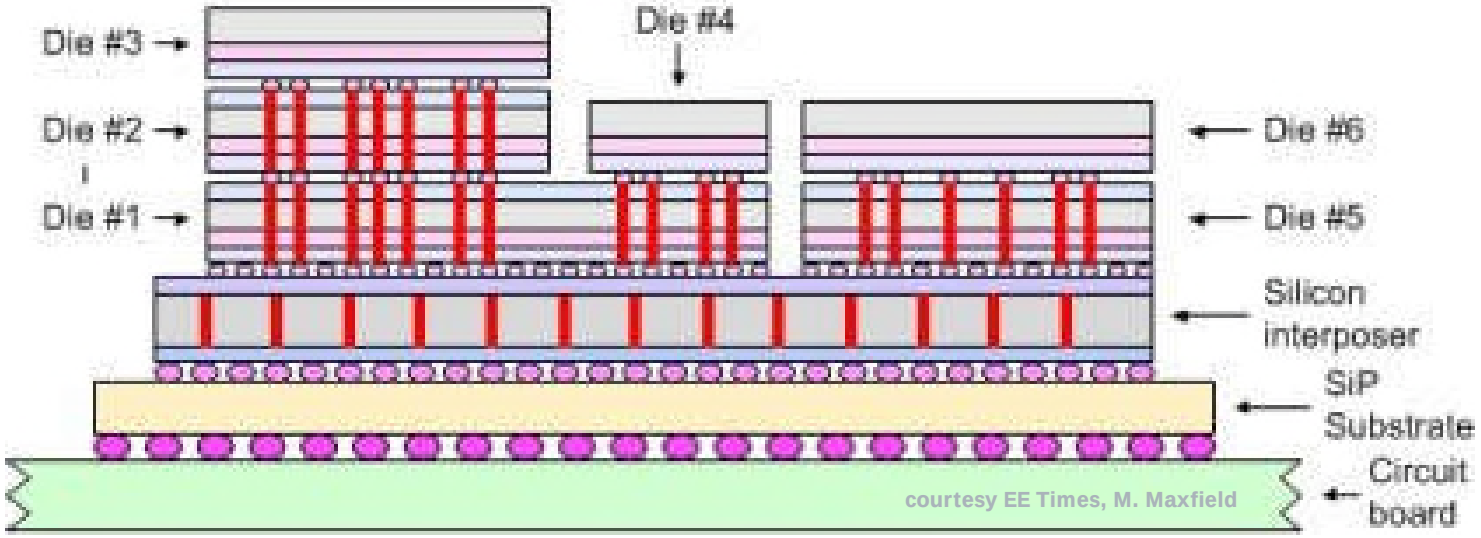
3D System-in-Package Technology



- *3D SiP technology represents highest density platform for integration at the package level among hetero and/or homogeneous devices*
  - Stacked die with through silicon via interconnects
  - High density integration between and among die stacks
  - Interposer technology with through silicon vias (or glass)

Organic Class Y SiP Technology Development

Cobham Collaborations with NASA NEPP/JPL

- Cobham and JPL have successfully collaborated on advanced flip chip technology development projects
  - Shared Cobham IR&D funding and JPL funding via NASA NEPP program
- Aeroflex Technology as Class-Y Demonstrator
  - Collaborative effort between Cobham (Aeroflex) and NEPP/JPL to study the reliability of Cobham flip chip technology as a Class Y demonstrator
  - Completed October 2014; JPL Publication 14-16 9/14
- Flip Chip on Organic Feasibility Study
  - Collaborative effort between Cobham and NEPP/JPL to study the feasibility of flip chip on organic technology for space applications
  - Completed March 2017; JPL Publication in progress
- *Fine Pitch Flip Chip on Organic Development*
  - Collaboration between Cobham and NEPP/JPL to evaluate the reliability of fine pitch flip chip on organic technology for space applications
  - *Commenced March 2017; September 2018 completion target*

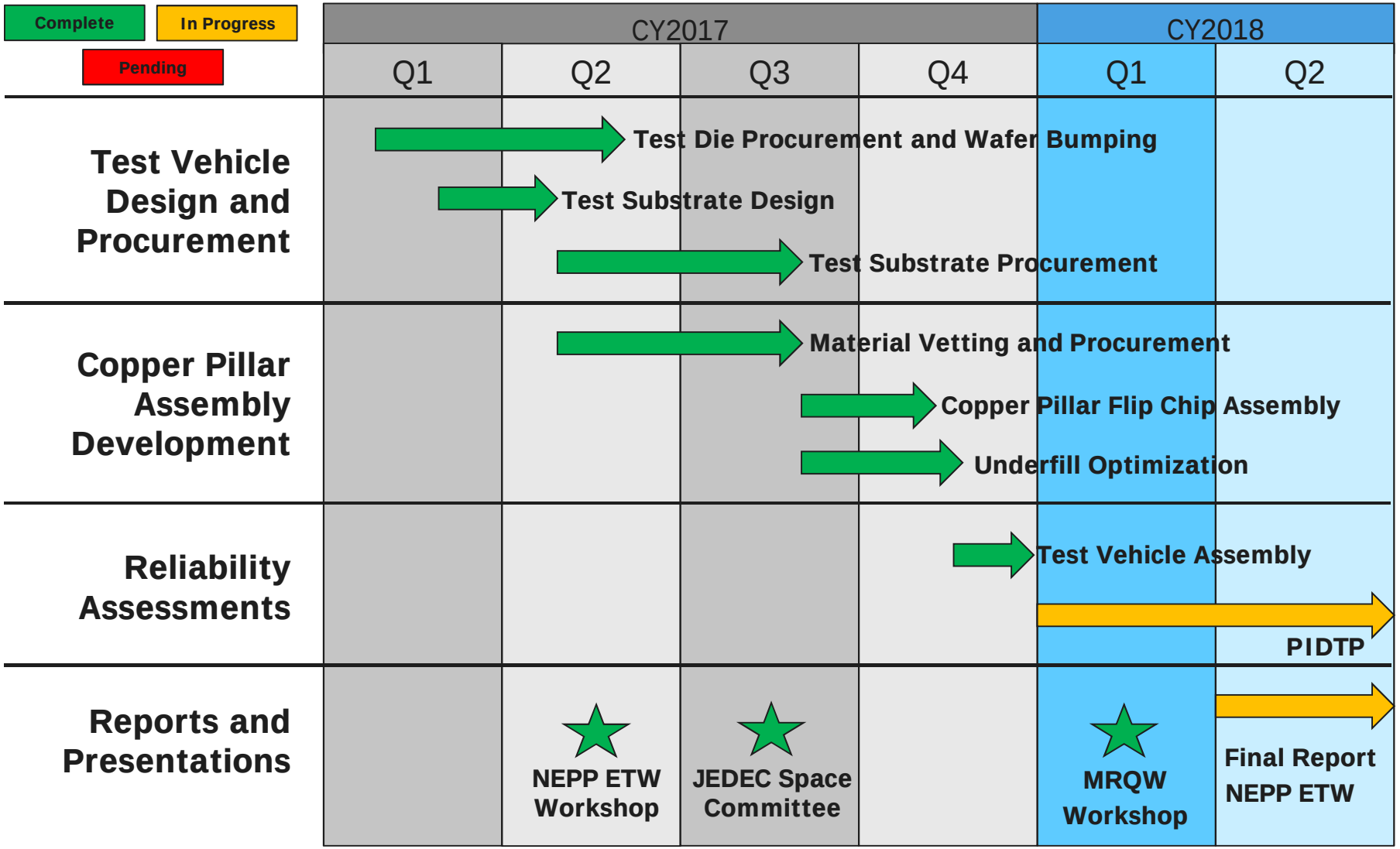
Fine Pitch Flip Chip on Organic Development

Objectives and Tasks

- *Objective: Evaluate the reliability of fine pitch flip chip on organic technology for high reliability and space applications*
  - Technical leads: Scott Popelar, Rich Measmer, Julie Hook, Jong-ook Suh (JPL)
  - Duration: March 2017 thru September 2018
- *Test Vehicle Design and Procurement*
  - Procure fine pitch (150µm) daisy chain test vehicle from Practical Components
  - Design and procure daisy chain HDBU organic test substrate from Kyocera
  - Evaluate supply chain for eutectic Sn/Pb copper pillar wafer bumping
- *Copper Pillar Assembly Development*
  - Vet flux and underfill material options for copper pillar assembly
  - Develop copper pillar flip chip assembly processes
  - Optimize underfill process with respect to voiding, etc.
- *PIDTP Reliability Assessments*
  - Test vehicle assembly and assembly monitors
  - Assess fine pitch copper pillar flip chip on organic reliability
    - Temperature Cycle Testing, High Temp Storage, Multiple Reflow, Moisture Loading

Fine Pitch Flip Chip on Organic Development

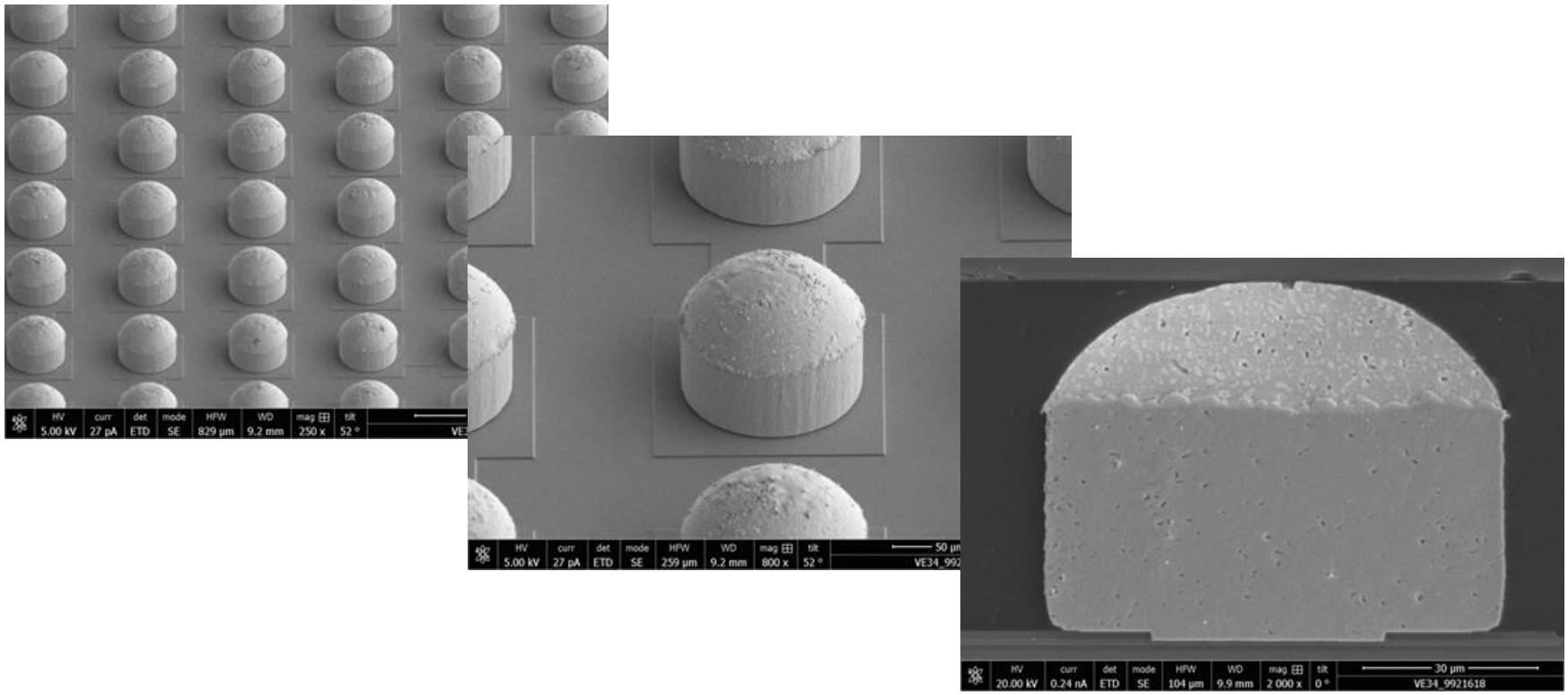
Milestone Schedule and Status



Fine Pitch Flip Chip on Organic Development

Test Vehicle Design and Procurement

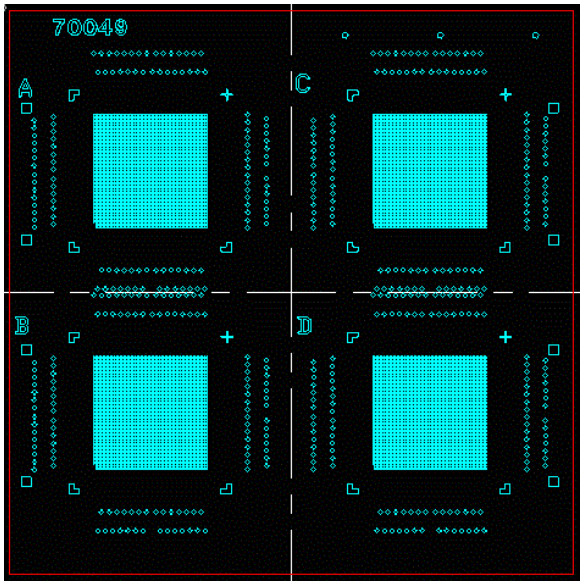
- *FC150 Flip Chip Daisy Chain Test Die*
  - 150µm I/O pitch daisy chain test vehicle
  - 10x10mm (3,718 I/O) and 20x20mm (14,872 I/O) die sizes
  - 40µm copper pillar bump, 25µm eutectic Sn/Pb solder cap

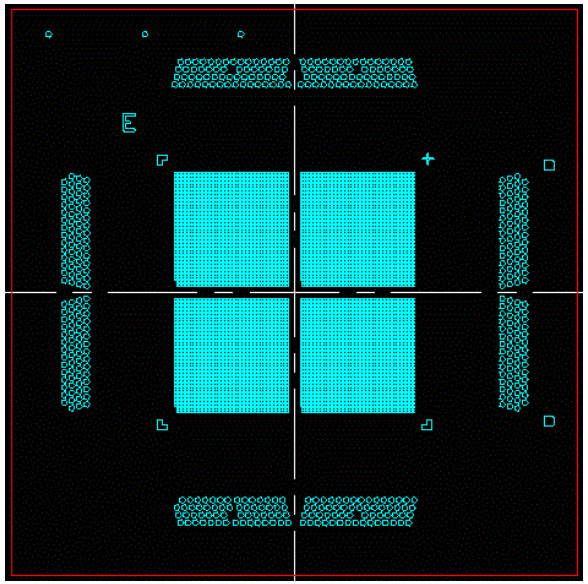


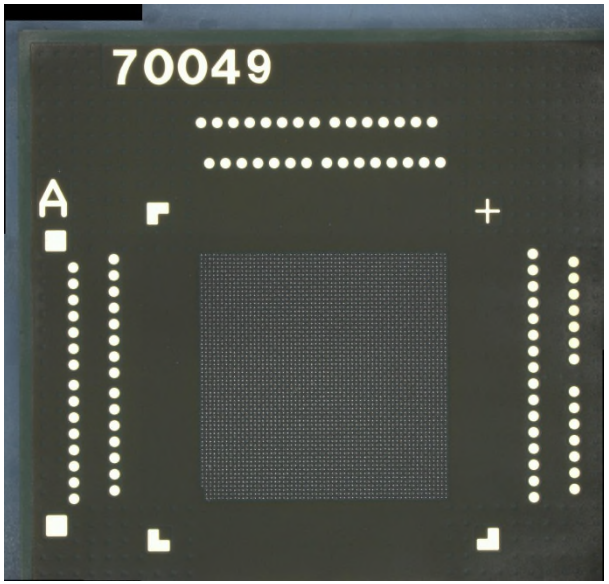
Fine Pitch Flip Chip on Organic Development

Test Vehicle Design and Procurement

- *Organic High Density Build-Up (HDBU) Test Substrate*
  - Dual-sided, 1.0mm thick, 45x45mm substrate size
  - 80µm solder mask defined pads with ENIG plating and eutectic SOP
  - Four 10x10mm die sites; single 20x20mm die site



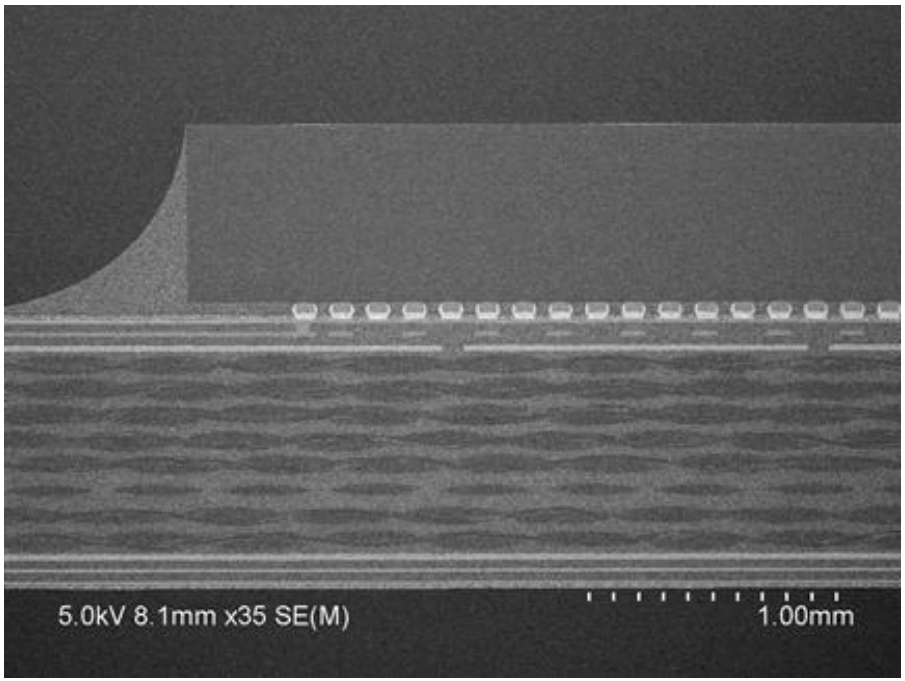


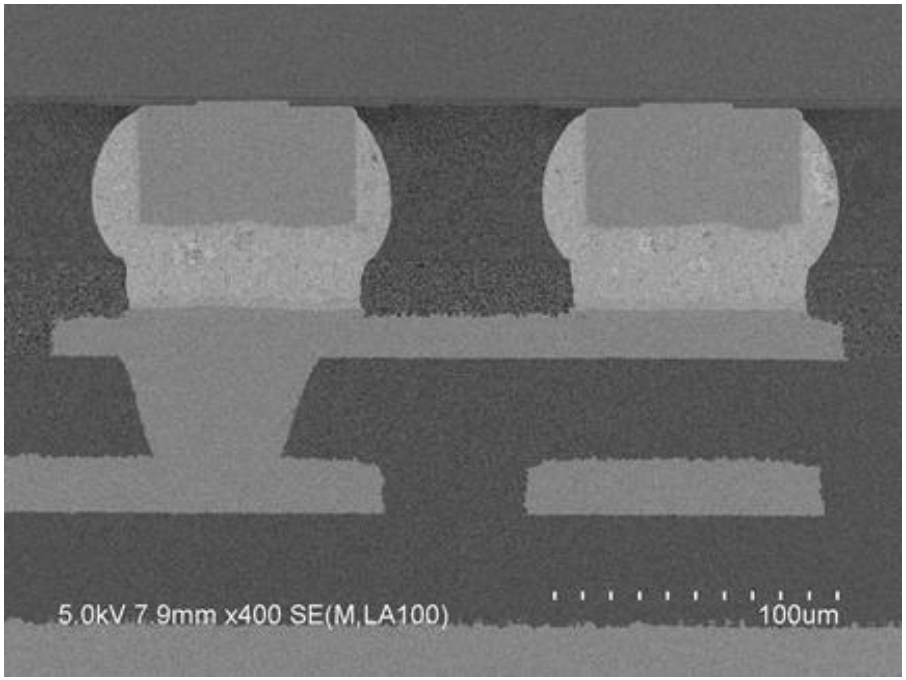


Fine Pitch Flip Chip on Organic Development

Copper Pillar Assembly Development

- *FC150 Assembly Monitor – Cross Section SEM*
  - Excellent solder joint wetting and formation

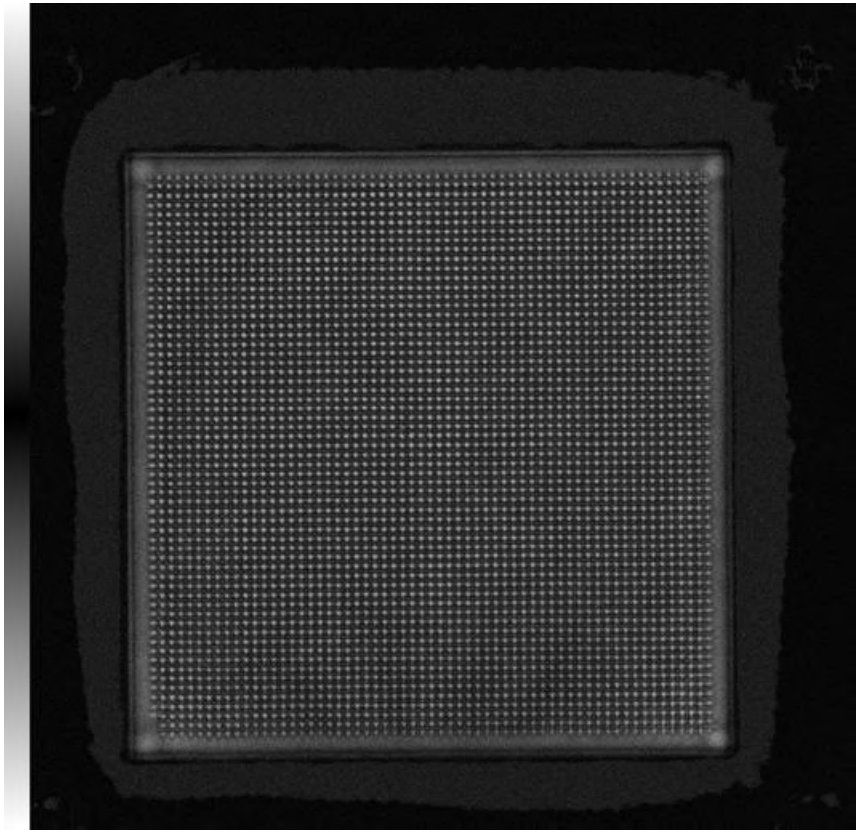


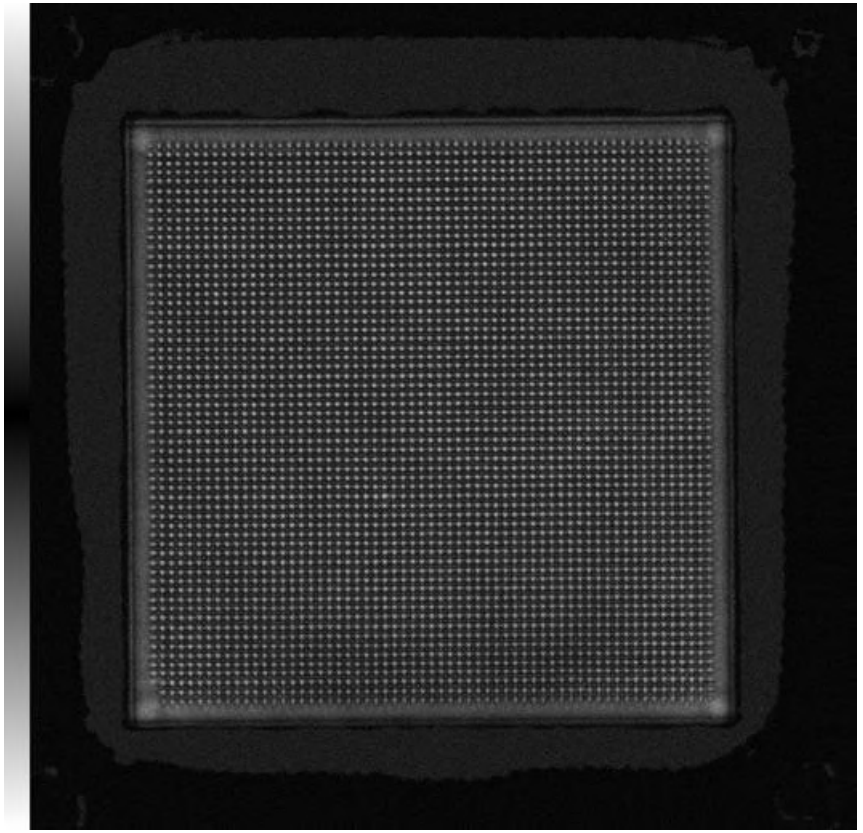


Fine Pitch Flip Chip on Organic Development

Underfill Assembly Development

- *FC150 Assembly Monitor – CSAM Underfill Inspection*
  - No underfill voids detected (10x10mm die)





Fine Pitch Flip Chip on Organic Development

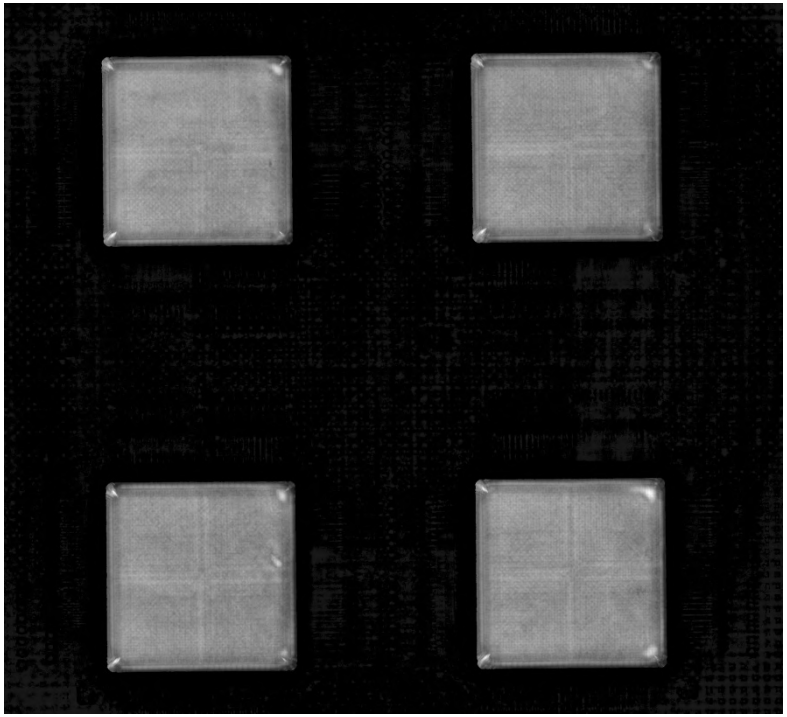
PIDTP Reliability Assessments

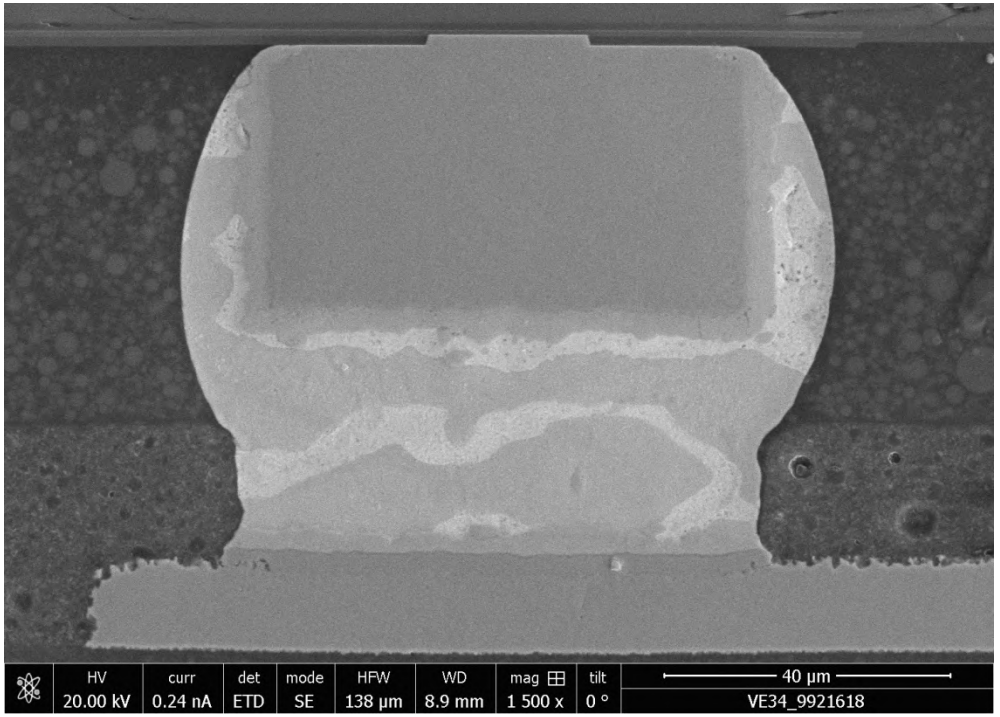
- *Condition B Temperature Cycle Testing (-55/125°C)*
  - Parts assembled with underfill; 10x10mm die size
  - *4500 cycles, no failures detected to date*
  - Test to 5000 cycles cumulative
- *125°C High Temperature Storage*
  - Parts assembled with underfill; 10x10mm die size
  - *2500 hours, no failures detected to date*
  - Test to 4000 hours cumulative
- *150°C High Temperature Storage*
  - Parts assembled with underfill; 10x10mm die size
  - *2500 hours, no failures detected to date*
  - Test to 4000 hours cumulative
- *Multiple Reflow Testing*
  - Parts assembled with underfill; 10x10mm die size
  - *10 reflow exposures, no failures detected*

Fine Pitch Flip Chip on Organic Development

PIDTP Reliability Assessments

- *Condition B Temperature Cycle Testing (-55/125°C)*
  - CSAM and Cross section analysis after 4000 cycles (zero failures)
  - No indication of underfill delamination; no evidence of underfill voids
  - Significant grain coarsening within solder joint (expected)

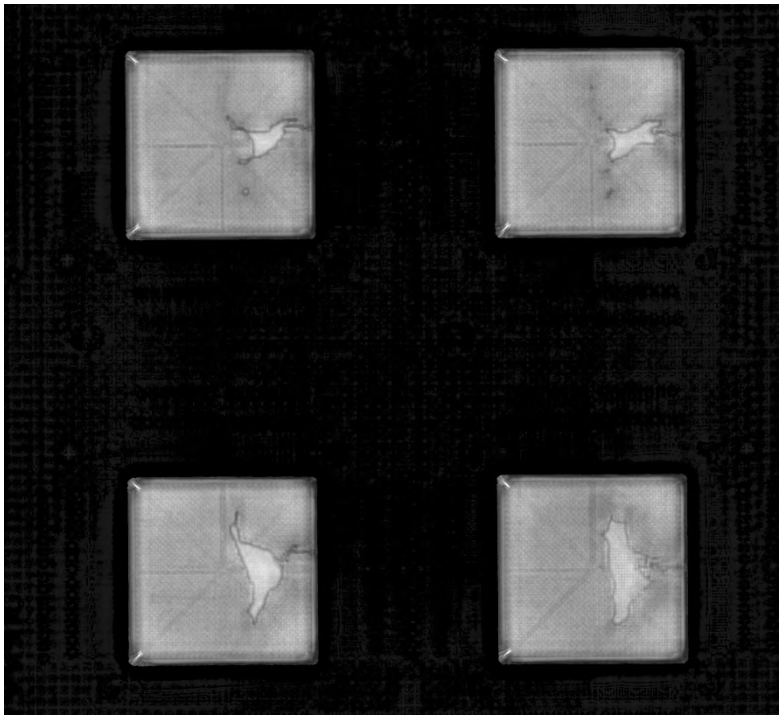


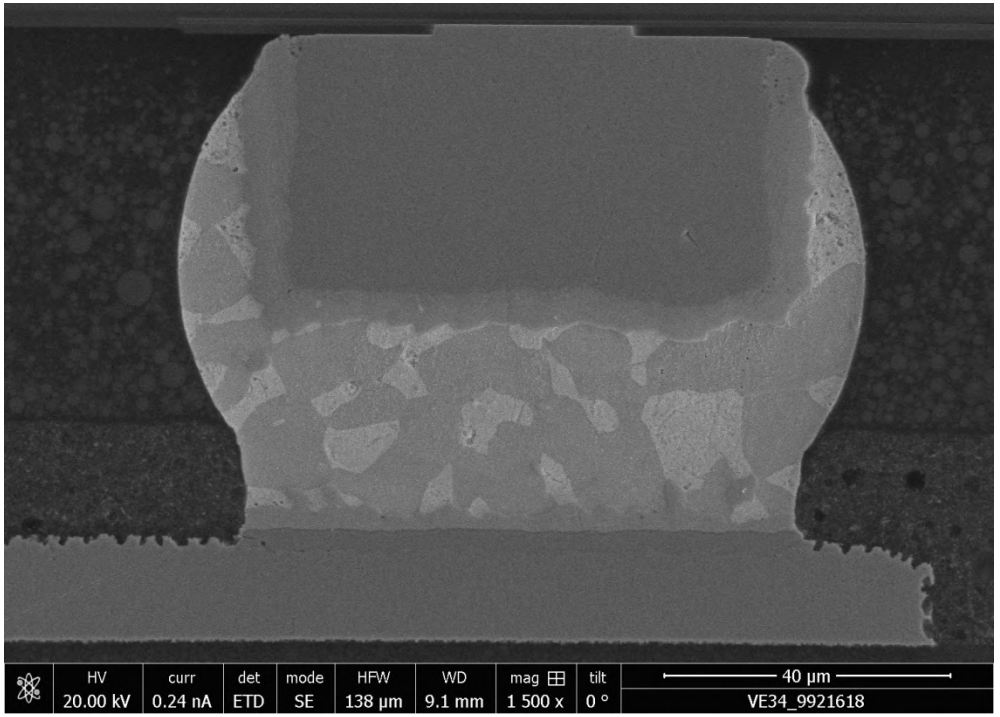


Fine Pitch Flip Chip on Organic Development

PIDTP Reliability Assessments

- *125°C High Temperature Storage*
  - CSAM and Cross section analysis after 2000 hours (zero failures)
  - No indication of underfill delamination; some evidence of underfill voids
  - Grain coarsening within solder joint and IMC growth (expected)

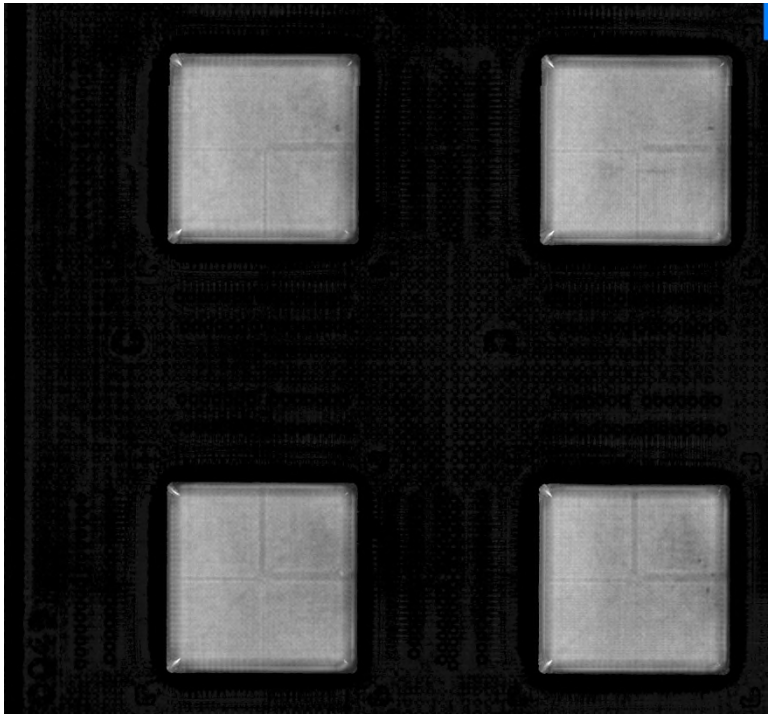


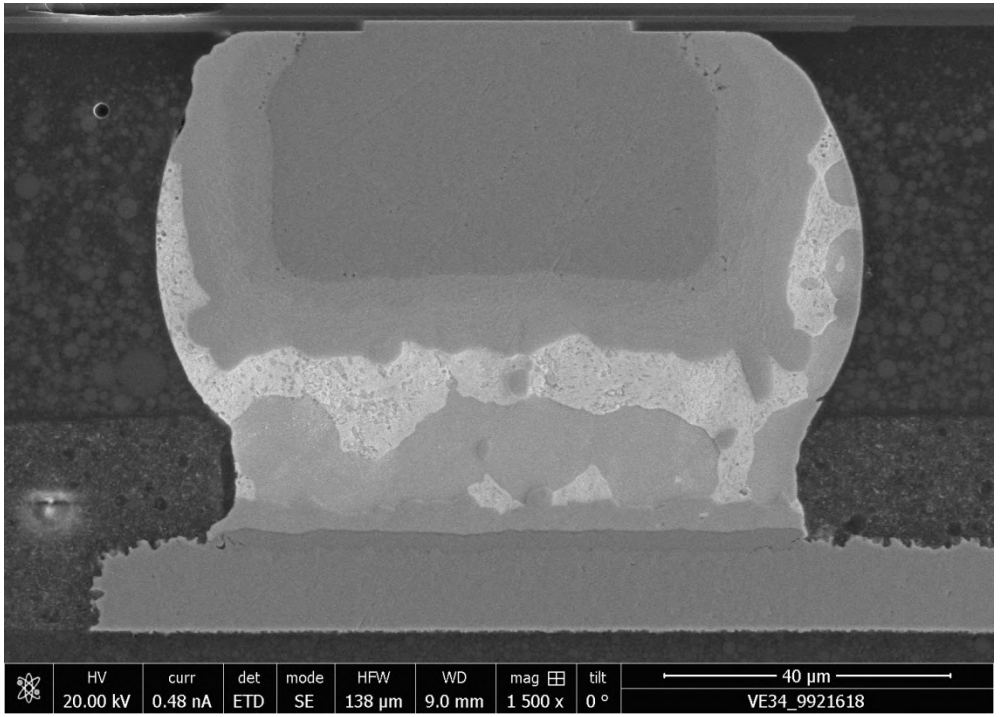


Fine Pitch Flip Chip on Organic Development

PIDTP Reliability Assessments

- *150°C High Temperature Storage*
  - CSAM and Cross section analysis after 2000 hours (zero failures)
  - No indication of underfill delamination; no evidence of underfill voids
  - Significant grain coarsening within solder joint and IMC growth (expected)





System-in-Package Technology Development

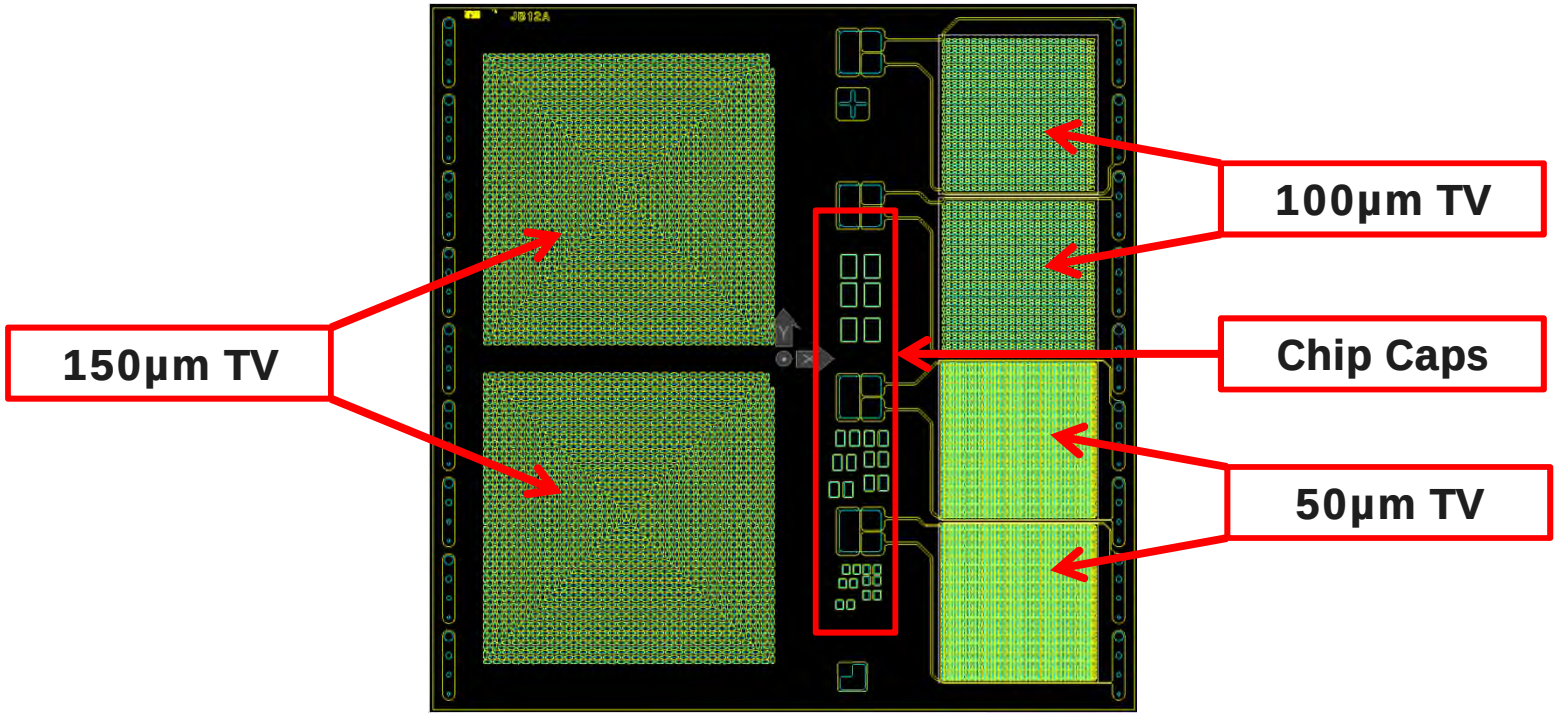
Objectives and Tasks

- *Objective: Provide the reliability baseline and foundation for design, fabrication and assembly of high reliability SiP solutions utilizing 2.5D interposer technology*
  - Technical Leads: Scott Popelar, Sean Thorne, Mike Newman, Rich Measmer, Julie Hook
  - Duration: January 2018 thru December 2018; extend into 2019
- *Test Vehicle Design and Procurement*
  - Design and procure test vehicles that enable the evaluation and development of 2.1D and 2.5D SiP technology
    - Silicon Interposer, Flip Chip Test Die, 2.1D Organic Substrate, 2.5D Silicon Interposer
- *Interposer Assembly Development*
  - Wafer bumping of test vehicles; ENIG plating and copper pillar bumping
  - Silicon interposer assembly development; flip chip assembly and underfill
- *Interposer Assembly Feasibility Demonstration*
  - Demonstration of Minimum Viable Product (MVP)
  - Perform baseline reliability assessments demonstrating feasibility of 2.5D technology
- *Technical Conference Participation*
  - Attend SiP technical conferences and workshops; publish as appropriate

System-in-Package Technology Development

Silicon Interposer Test Vehicle Design and Procurement

- *JB12A Silicon Interposer Test Vehicle*
  - Daisy chain assembly sites for 50, 100 and 150µm daisy chain test vehicles
  - Assembly sites for 01005, 0201 and 0402 chip caps
  - Embedded pads for subsequent attachment to organic substrate
  - *Wafers received from Fab; ENIG plating complete*

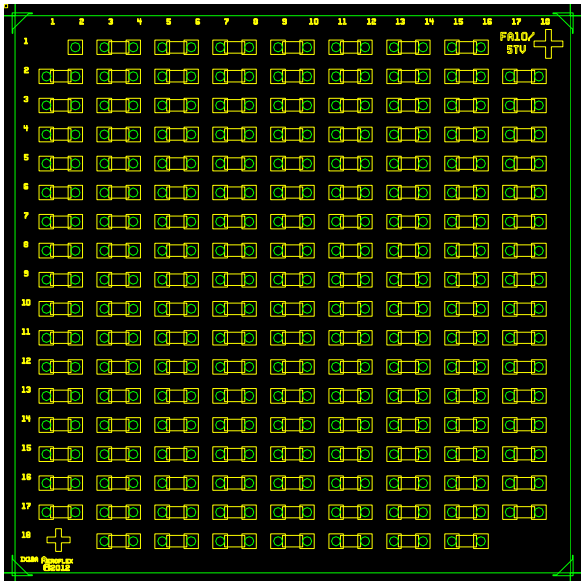


System-in-Package Technology Development

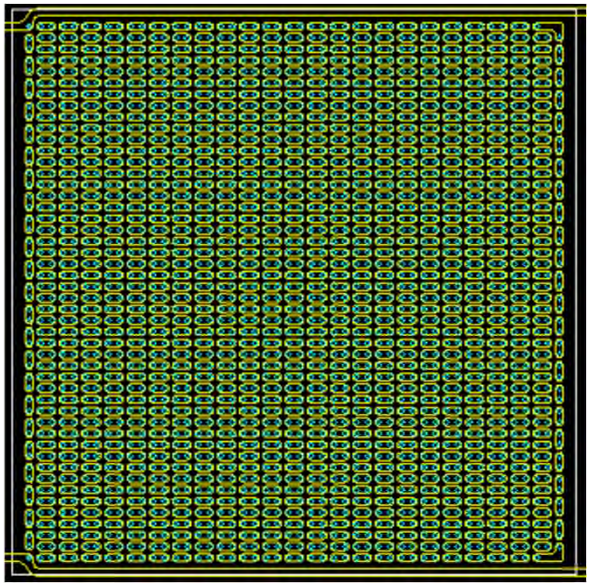
Fine Pitch Flip Chip Test Vehicle Design and Procurement

- *JB13A and JB14A Fine Pitch Daisy Chain Test Vehicles*
  - 100 and 50µm pitch test die in 5x5mm formats
  - *CDR completed with Fab; wafer fabrication to complete in mid-June*

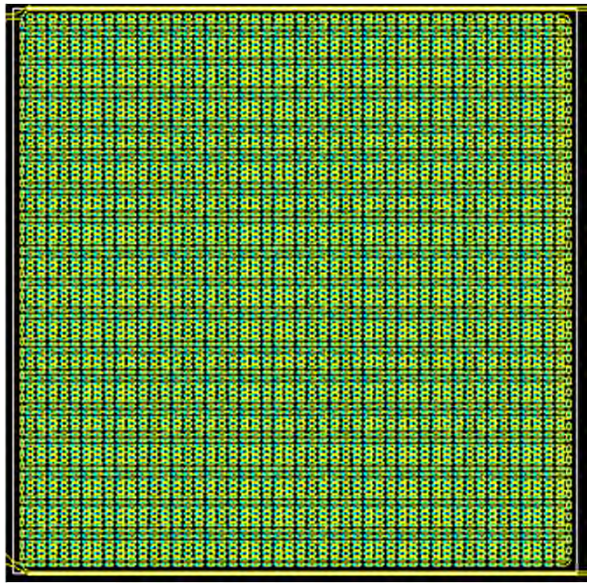
Physical comparison of I/O density versus pitch for 5x5mm die size



254µm pitch
317 I/O
(IX18A)



100µm pitch
2,300 I/O
(JB13A)

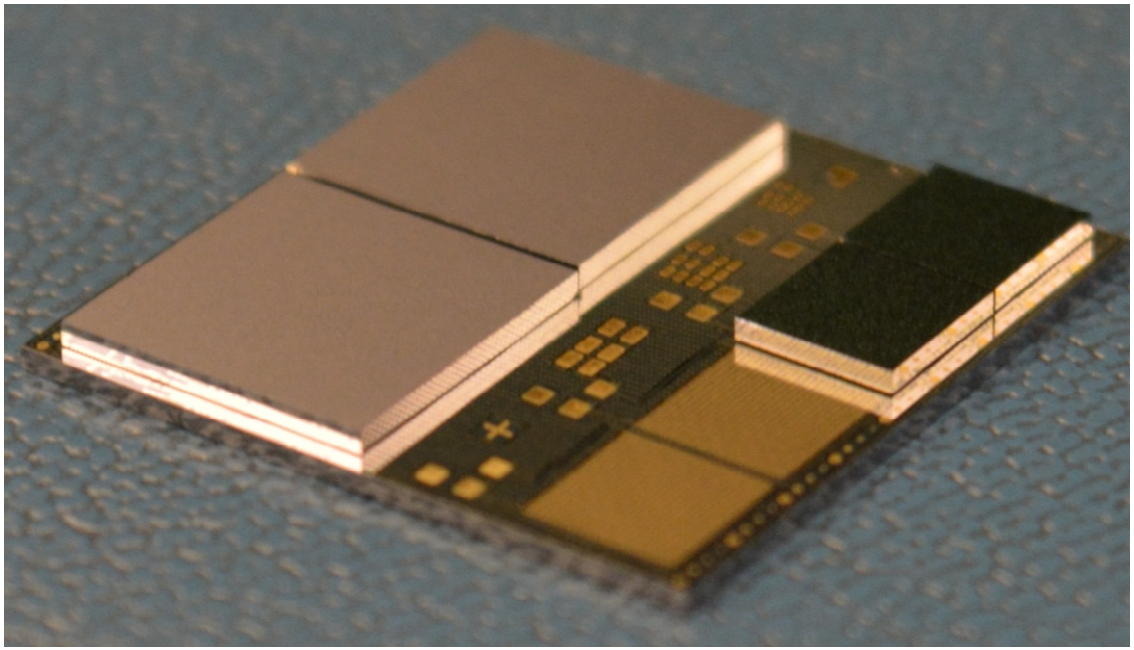


50µm pitch
9,600 I/O
(JB14A)

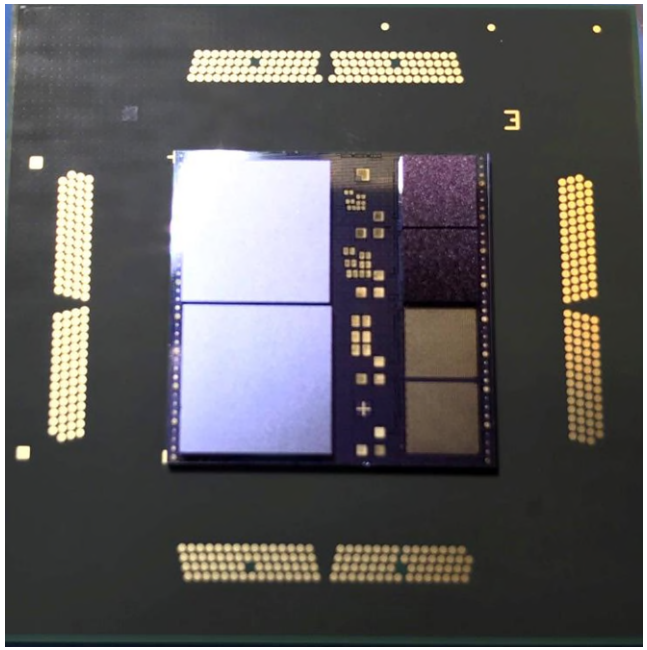
System-in-Package Technology Development

2.5D Test Vehicle Assembly Development

- *2.5D Minimum Viable Product (MVP) Technology Demonstrator*
  - Flip chip test vehicle assembly to silicon interposer
  - Silicon interposer assembly to organic substrate



Silicon Interposer Assembly

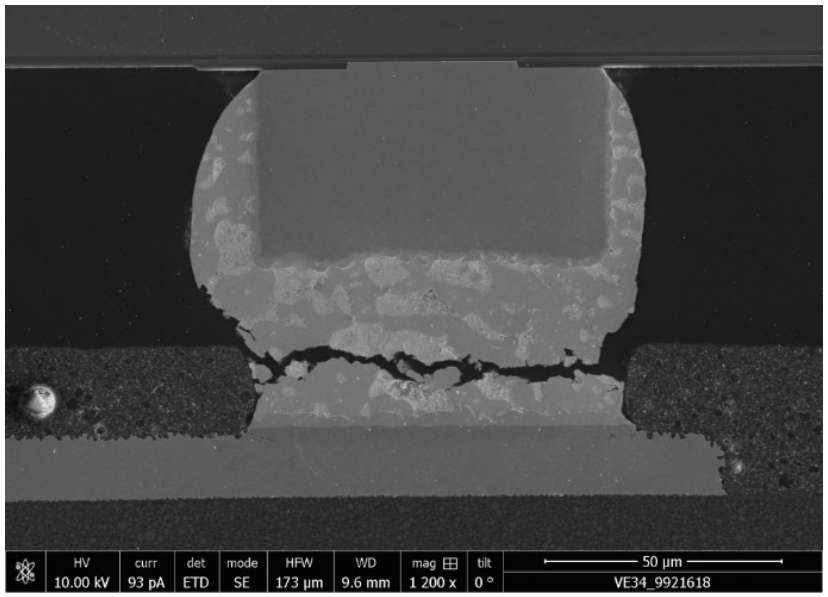


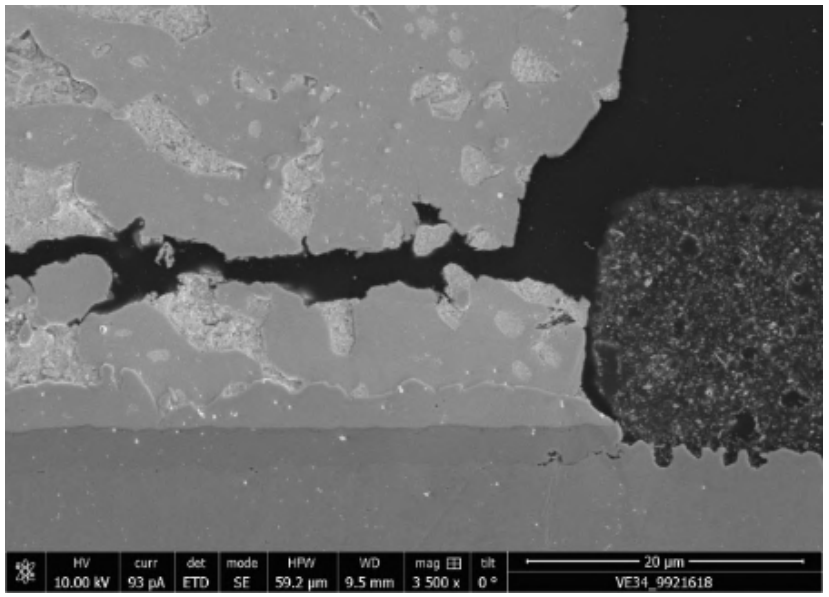
Organic Substrate Assembly

Physics-of-Failure Reliability Modeling

Solder Fatigue Failure Mechanism

- *Slow Ramp Rate Temperature Cycle Testing – No Underfill*
  - FC150 assemblies without underfill; ensure early failure due to CTE mismatch
  - Mild 0/100°C and 25/125°C temperature profiles evaluated
  - Confirmed solder fatigue failure mode in copper pillar interconnect
  - *Incorporate results into solder fatigue correlation*

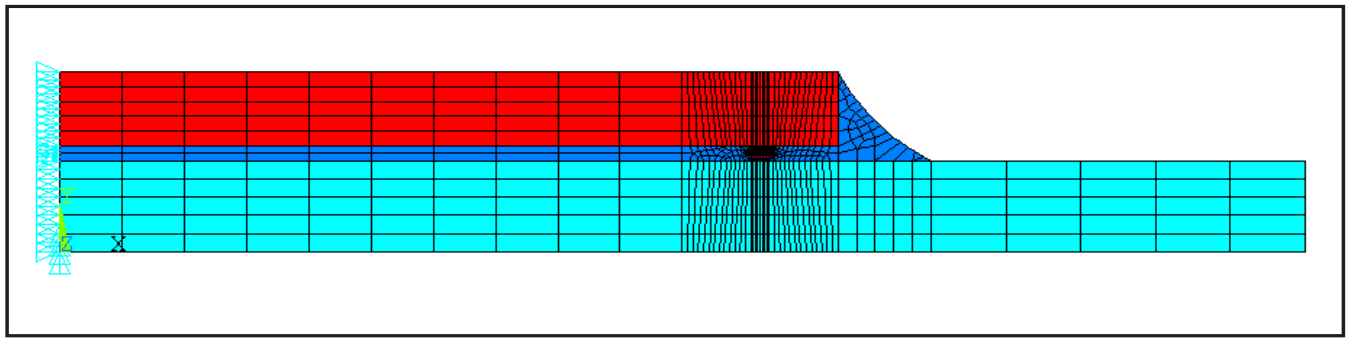


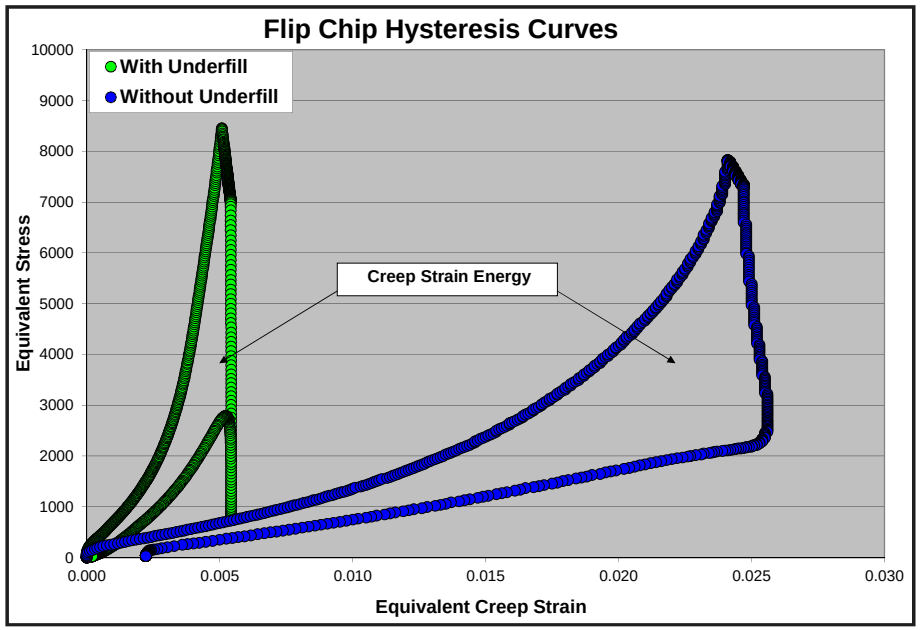


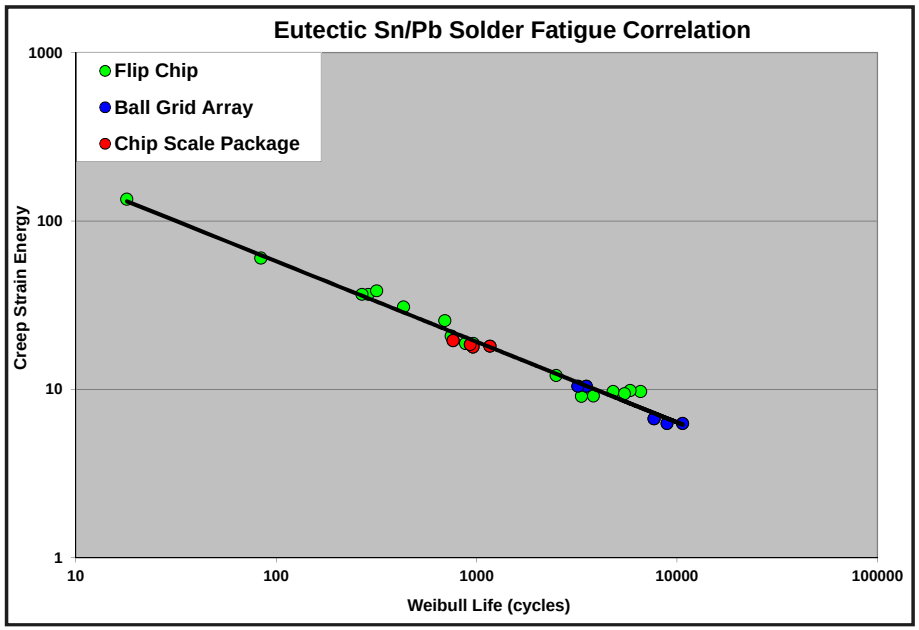
Physics-of-Failure Reliability Modeling

Solder Fatigue Modeling – Weibull Life Fatigue Prediction

ANSYS Mechanical -> Finite Element Analysis -> Solder Fatigue Correlation







Physics-of-Failure Reliability Modeling

Solder Fatigue Modeling – De-rating to Use Conditions

- *De-rating to Use Conditions*
  - Modified Coffin-Manson Equation (Norris-Landzberg, IBM 1969)

$$AF = \left(\frac{\Delta T_{test}}{\Delta T_{use}}\right)^{\gamma} \times \left(\frac{f_{use}}{f_{test}}\right)^{\frac{1}{3}} \times e^{\left(\frac{E_a}{k_b}\left[\frac{1}{T_{\max,\,use}} - \frac{1}{T_{\max,\,test}}\right]\right)}$$

$$Cycles_{use} = AF \times Cycles_{test}$$

- *2-parameter Weibull Distribution*

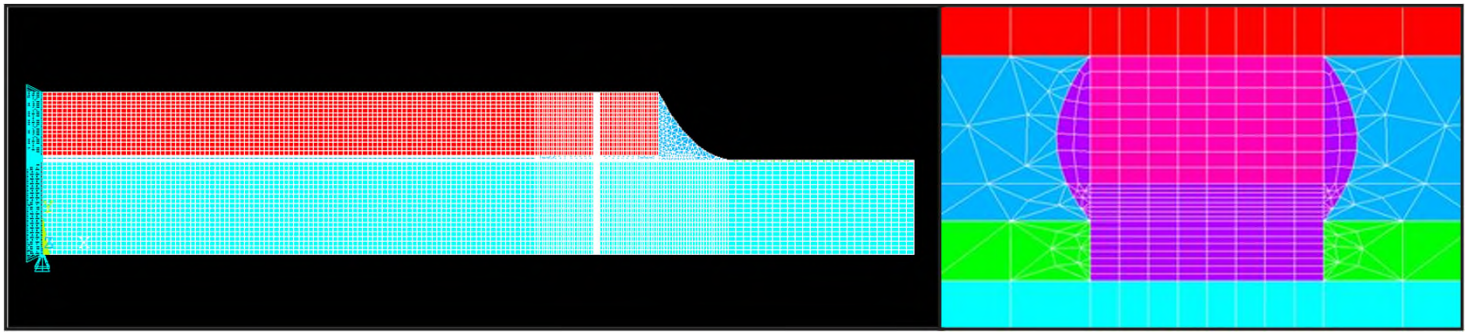
$$F(x) = 1 - e^{-(x/\theta)^{\beta}}$$

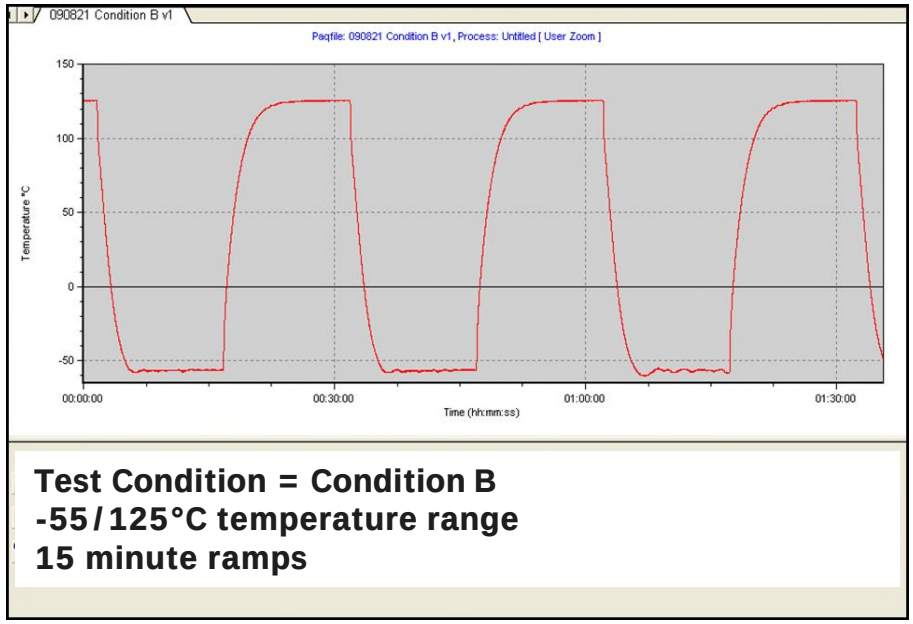
  - $F(x)$ = Cumulative failure distribution; probability of failure at x number of cycles
  - β = Weibull slope; indicative of failure mechanism (i.e., for solder fatigue, $\beta \approx 6$)
  - θ = Weibull life; defines number of cycles with 63.2% cumulative failures
  - Weibull distribution commonly used to characterize wearout failure mechanisms such as solder fatigue

Physics-of-Failure Reliability Modeling

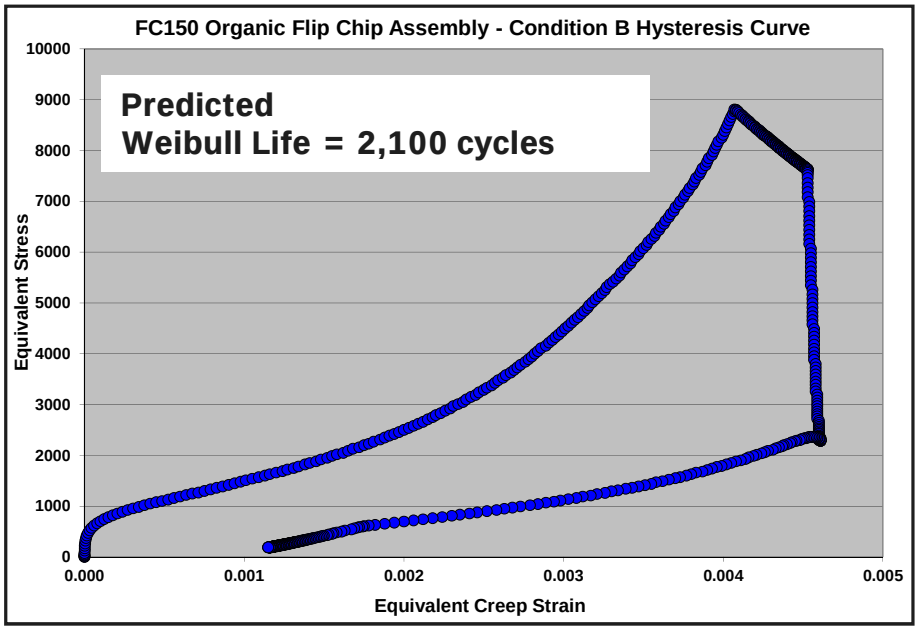
FC150 on Organic Substrate – Reliability Assessment

ANSYS Mechanical -> Finite Element Analysis -> Solder Fatigue Correlation





Test Condition = Condition B
-55/125°C temperature range
15 minute ramps



Physics-of-Failure Reliability Modeling

FC150 on Organic Substrate – Reliability Assessment

- *Predict Probability of No Failures for given Use Condition and Target Life*
  - Use Condition: 50/70°C, 2 cycles/day
  - Acceleration Factor: 62
  - Target Life: 20 years (14,600 cycles)
  - *Probability of No Failures: 99.9998%*

OR

- *Predict First Failure for given Use Condition and Confidence Level*
  - Use Condition: 40/55°C, 1 cycle/day
  - Acceleration Factor: 105
  - Confidence Level: 99.9999%
  - *First Failure: 22,630 cycles (62 years)*

Organic Class Y SiP Technology Development

Future Work

- Complete remaining Fine Pitch Flip Chip on Organic reliability assessments and generate final report
- Continue with 2.1D and 2.5D System-in-Package technology test vehicle and assembly development, and perform preliminary reliability assessments
- *Continue to engage the high reliability space community with respect to development, integration and implementation of System-in-Package technology*
- Further develop a Physics-of-Failure methodology to reliability modeling, with an initial focus on solder fatigue of copper pillar interconnects